

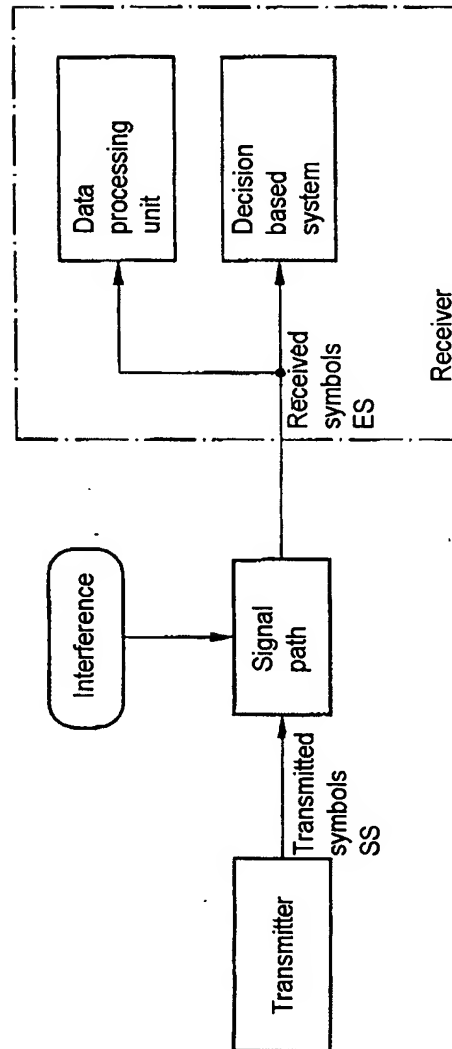


S3051

App. No. 10/799,346
Missing Parts Dated: May 28, 2004
Response to Missing Parts Dated: July 28, 2004
Replacement Sheet

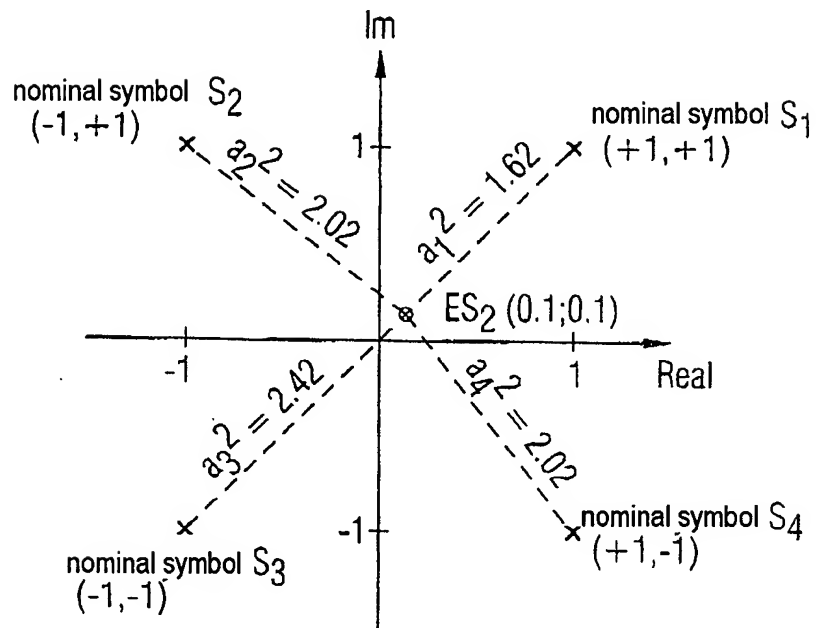
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FIG 1
Prior art



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FIG 2
Prior art



$$\text{Min} \{ a_i^2 \} = \text{Min} \{ 1.62; 2.02; 2.42; 2.02 \} = 1.62$$

4 nominal symbols

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FIG 3

Prior art

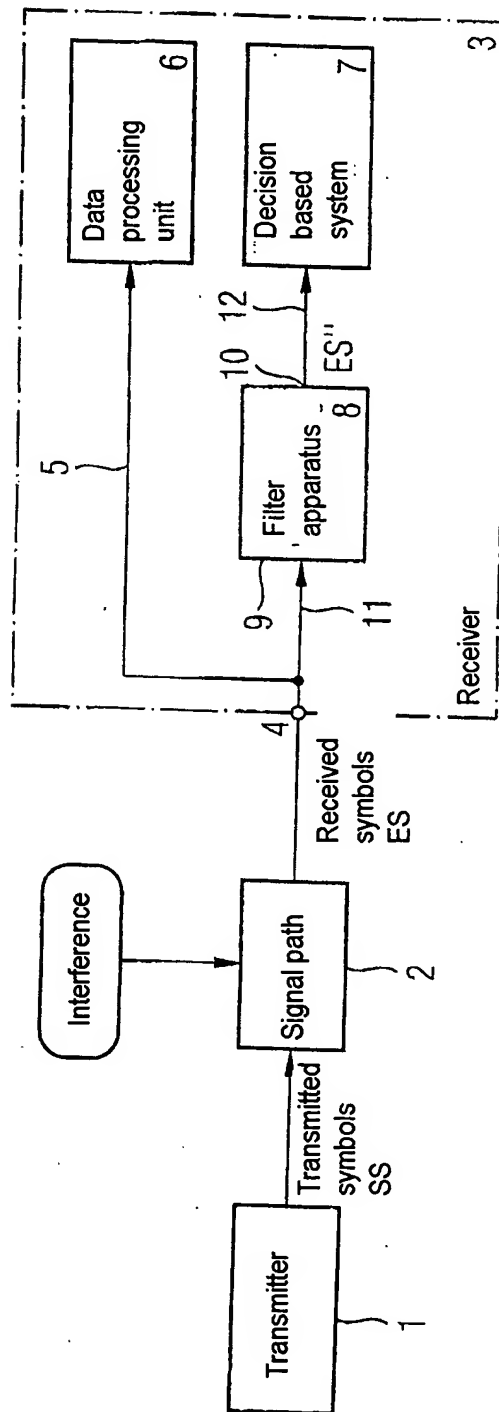
Example:

Transmitted symbol sequence (SS)		SS1	SS2	SS3	SS4	SS5	SS6
	Re	+1	-1	+1	-1	+1	+1
	Im	+1	+1	+1	-1	-1	-1
Received symbol sequence (ES)		ES1	ES2	ES3	ES4	ES5	ES6
	Re	1.5	0.1	0.4	-0.6	1.1	0.8
	Im	0.8	0.1	0.2	-0.1	-0.9	-2
Interval Min { a_i^2 } a_i^2 (min)		0.29	1.62	1	0.97	0.02	1.04
Decision (ES)		ES1	ES2	ES3	ES4	ES5	ES6
	Re	+1	+1	+1	-1	+1	+1
	Im	+1	+1	+1	-1	-1	-1

Table

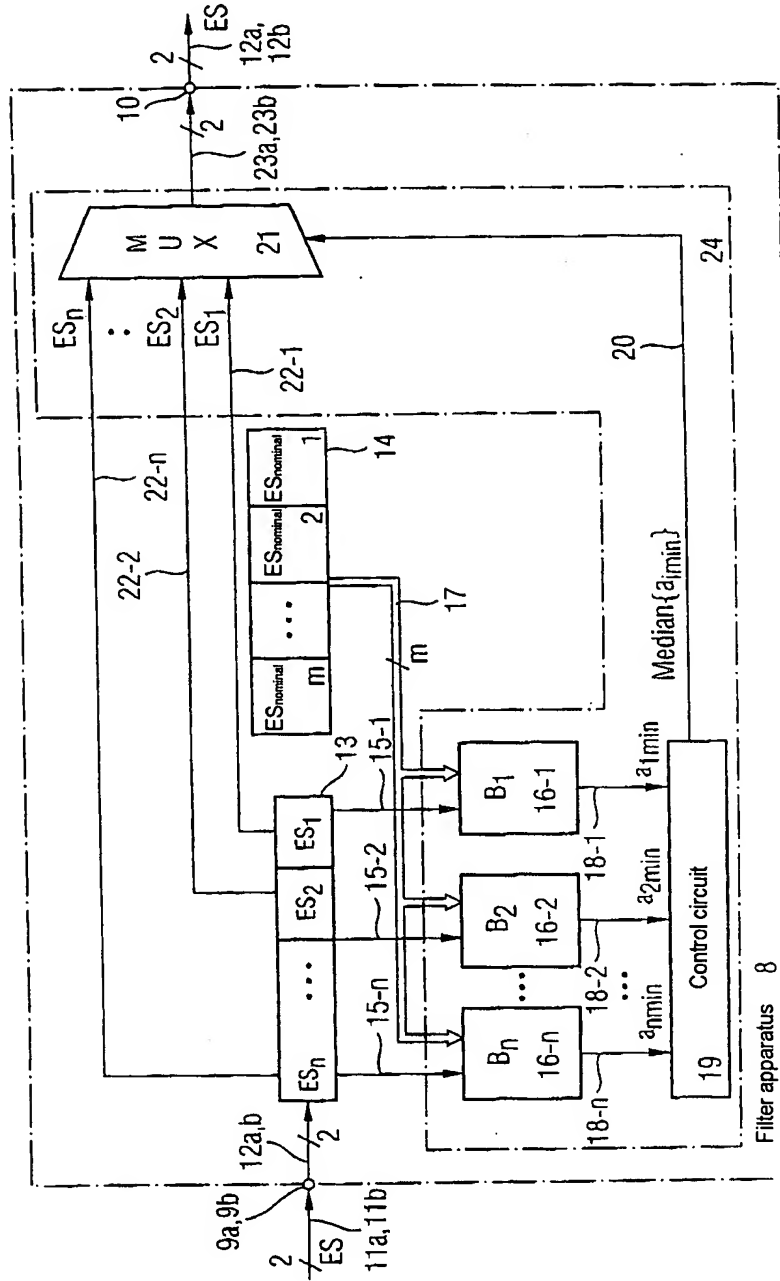
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FIG 4



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FIG 5

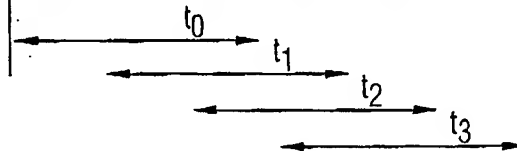


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FIG 6

Example:

		SS1	SS2	SS3	SS4	SS5	SS6
Transmitted symbol sequence (SS)	Re	+1	-1	+1	-1	+1	+1
	Im	+1	+1	+1	-1	-1	-1
		ES1	ES2	ES3	ES4	ES5	ES6
Received symbol sequence (ES')	Re	1.5	0.1	0.4	-0.6	1.1	0.8
	Im	0.8	0.1	0.2	-0.1	-0.9	-2



Interval Min { a_i^2 } (min)	0.29	1.62	1	0.97	0.02	1.04
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3-element groups :	t_0 (0.29 ; 1.62 ; 1)	→	1 (Pos3)
	t_1 (1.62 ; 1 ; 0.97)	→	1 (Pos2)
	t_2 (1 ; 0.97 ; 0.02)	→	0.97 (Pos2)
	t_3 (0.97 ; 0.02 ; 1.04)	→	0.97 (Pos1)

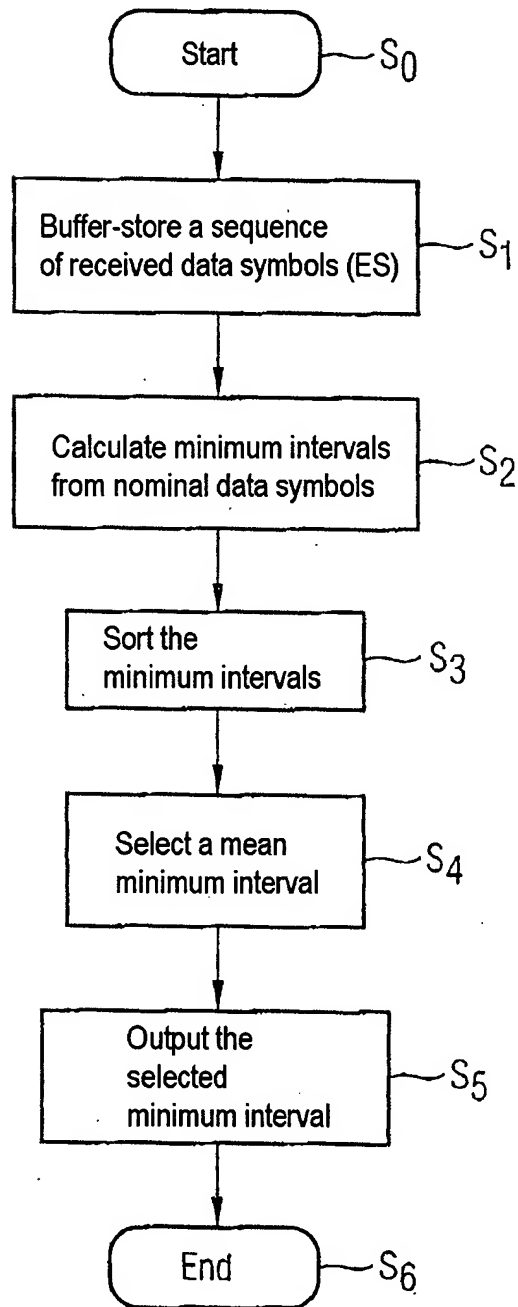
Sorted intervals Pos3 Pos2 Pos2 Pos1

		ES1'	ES2'	ES3'	ES4'
Filtered received symbol sequence (ES')	Re	0.4	0.4	-0.6	-0.6
	Im	0.2	0.2	-0.1	-0.1
		ES1	ES2	ES3	ES4
Decision E	Re	+1	+1	-1	-1
	Im	+1	+1	-1	-1

Table

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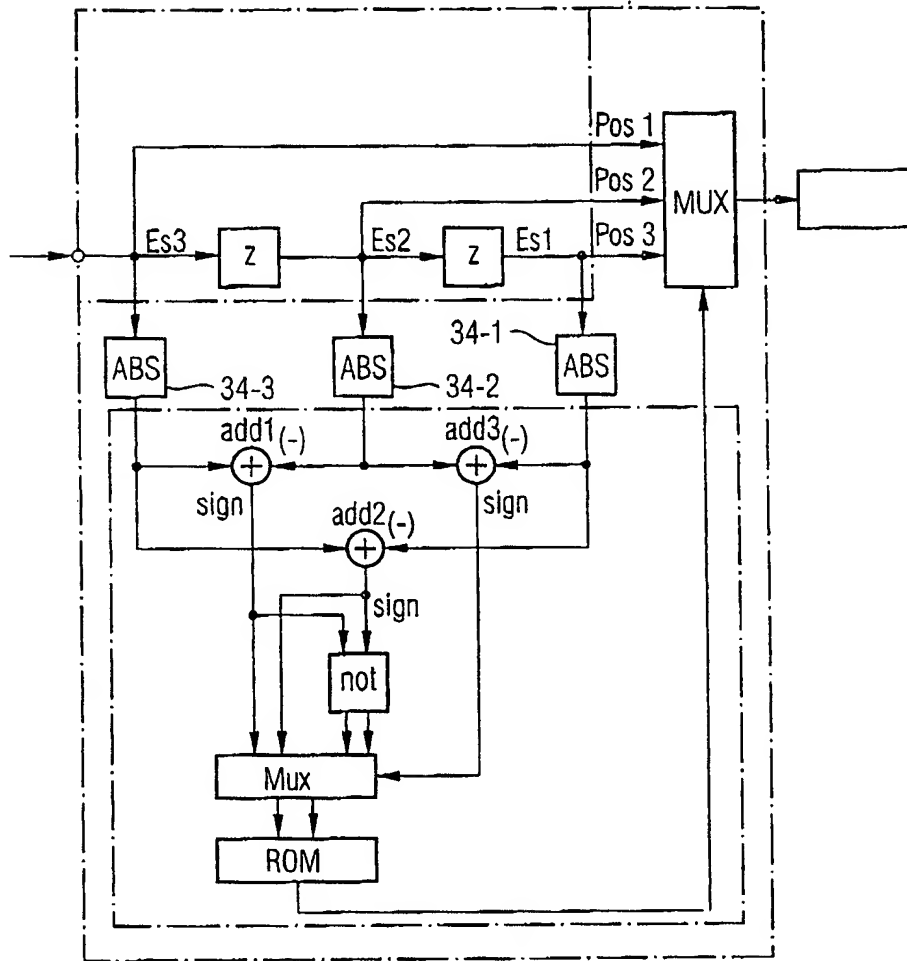
FIG 7



The diagram illustrates a control circuit 8, which is part of a larger system 10. The circuit is enclosed in a dashed box labeled 13. It processes a reference signal $Re(ES)$ through a feedback loop. The signal $Re(ES)$ is fed into a summing junction 26-3, which also receives a feedback signal from a multiplexer (MUX) 21. The output of 26-3 is processed by an absolute value block (ABS) 25-3. The output of 25-3 is fed into a summing junction 26-2, which also receives a nominal error signal $ES_{nominal}$. The output of 26-2 is processed by an absolute value block (ABS) 25-2. The output of 25-2 is fed into a summing junction 26-1, which also receives a nominal error signal $ES_{nominal}$. The output of 26-1 is processed by an absolute value block (ABS) 25-1. The outputs of the ABS blocks 25-3, 25-2, and 25-1 are fed into adders 28-1, 28-2, and 28-3, respectively. The outputs of the adders 28-1 and 28-2 are fed into a sign block (SIGN) 29-3. The output of the sign block 29-3 is fed into a NOT gate (32). The output of the NOT gate (32) is fed into a multiplexer (MUX) 31. The output of the MUX 31 is fed into a ROM (33). The ROM (33) is controlled by a control signal S (30) and a position signal Pos (20). The output of the ROM (33) is fed into a summing junction 28-3. The output of the summing junction 28-3 is fed into a sign block (SIGN) 29-1. The output of the sign block 29-1 is fed into a multiplexer (MUX) 21. The output of the MUX 21 is fed back to the summing junction 26-3. The circuit is also controlled by a control signal S (30) and a position signal Pos (20).

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FIG 9



[illegible]